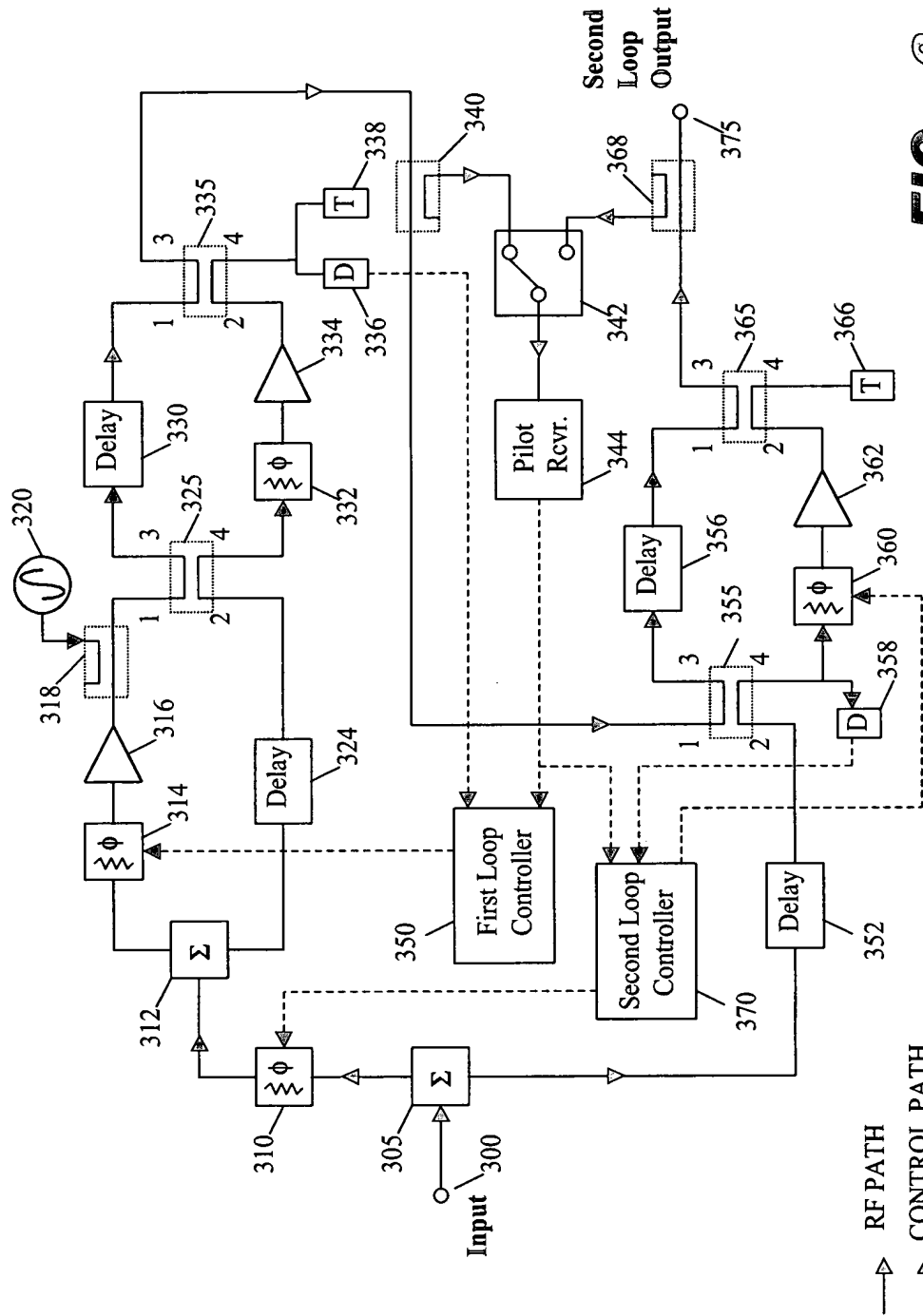
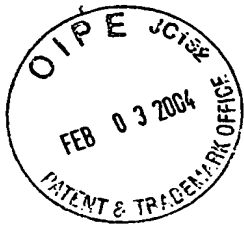


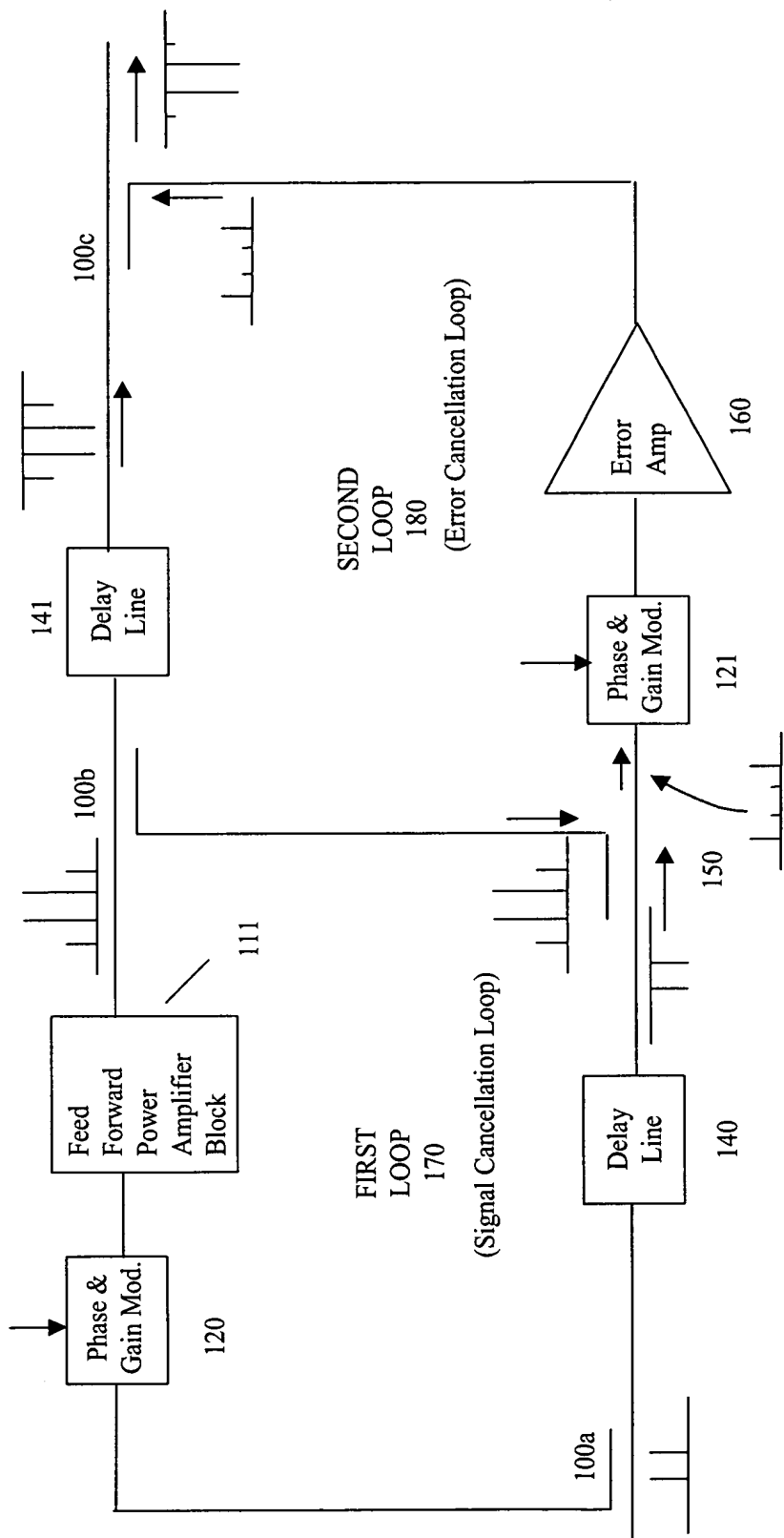
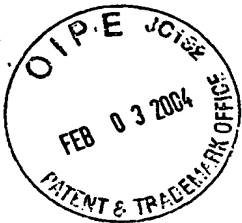
**FIG. 1**

PRIOR ART



**FIG. 2**

PRIOR ART



**FIG. 3**

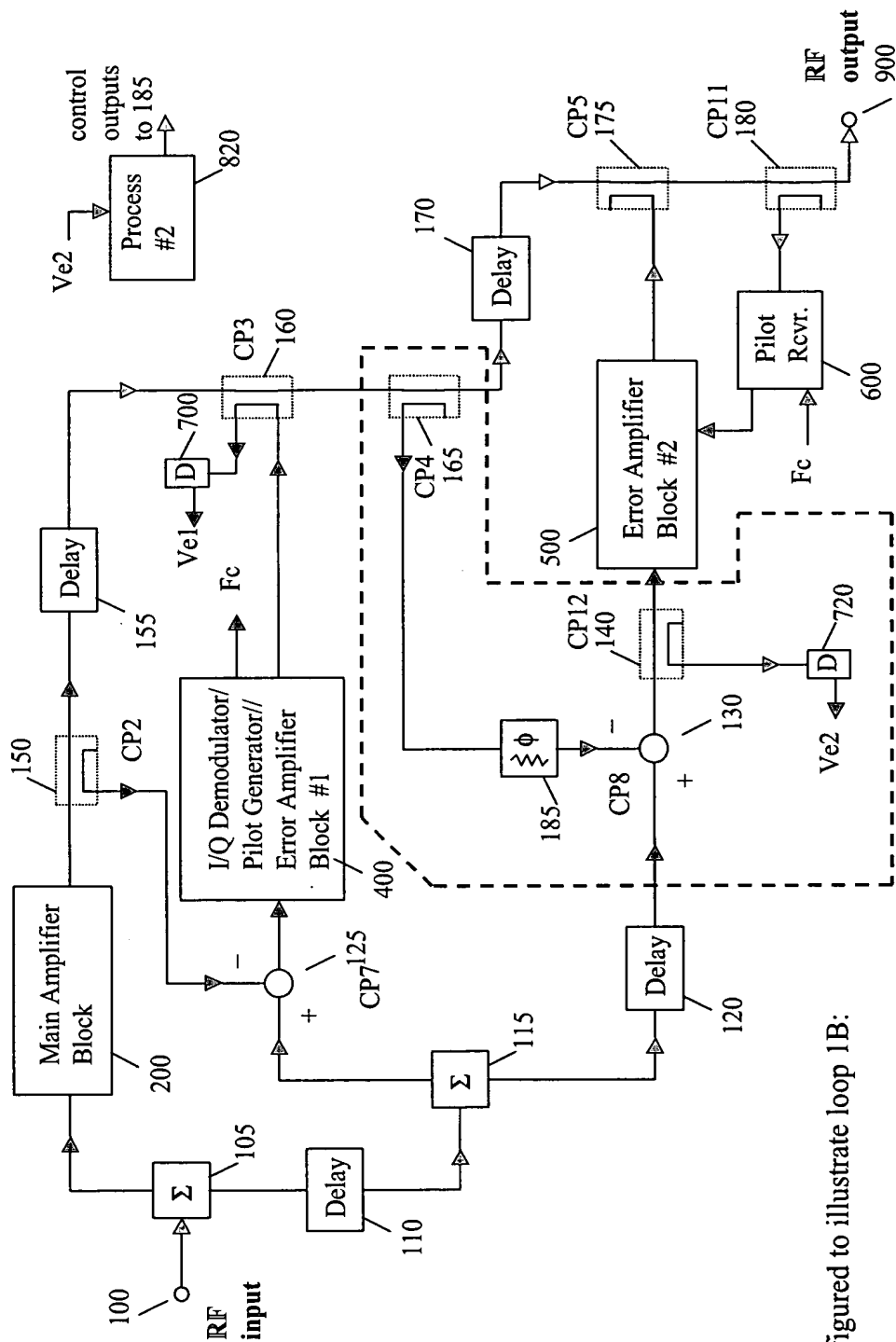
PRIOR ART



**FIG. 4**



**FIG. 5**

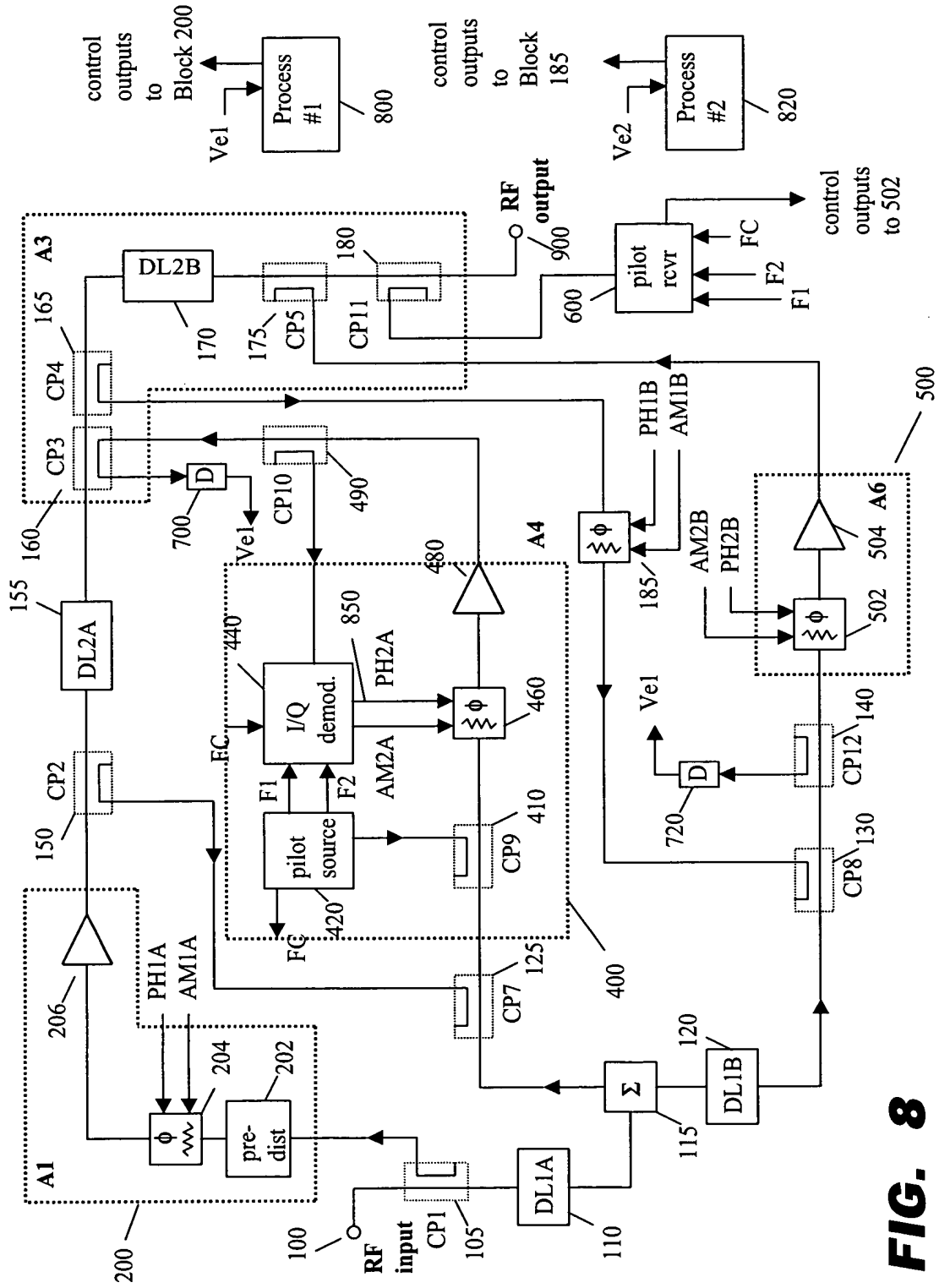
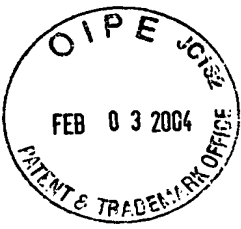


configured to illustrate loop 1B:

**FIG. 6**

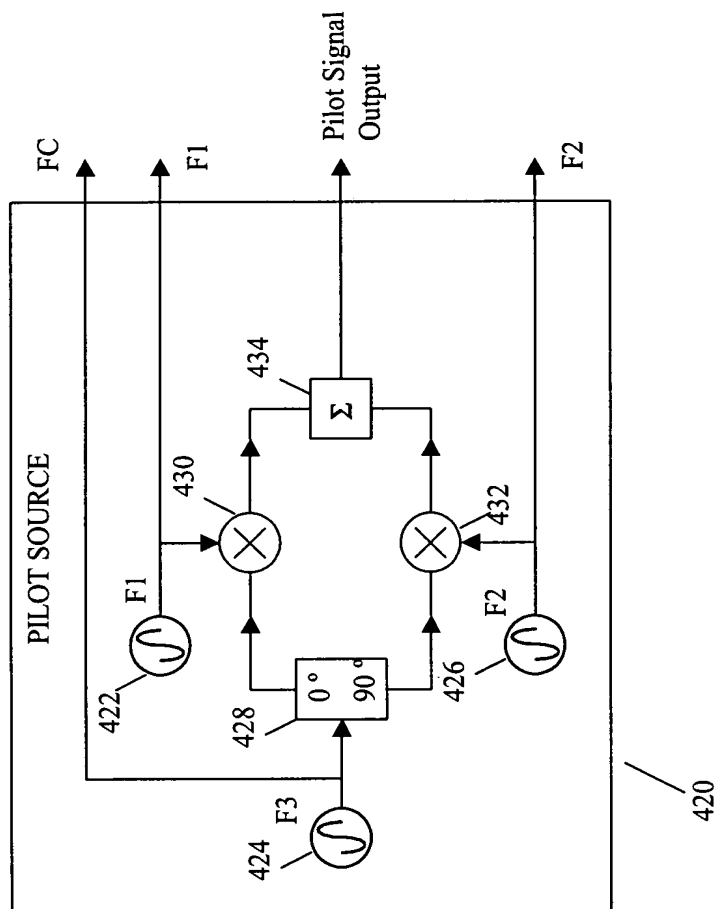


**FIG. 7**

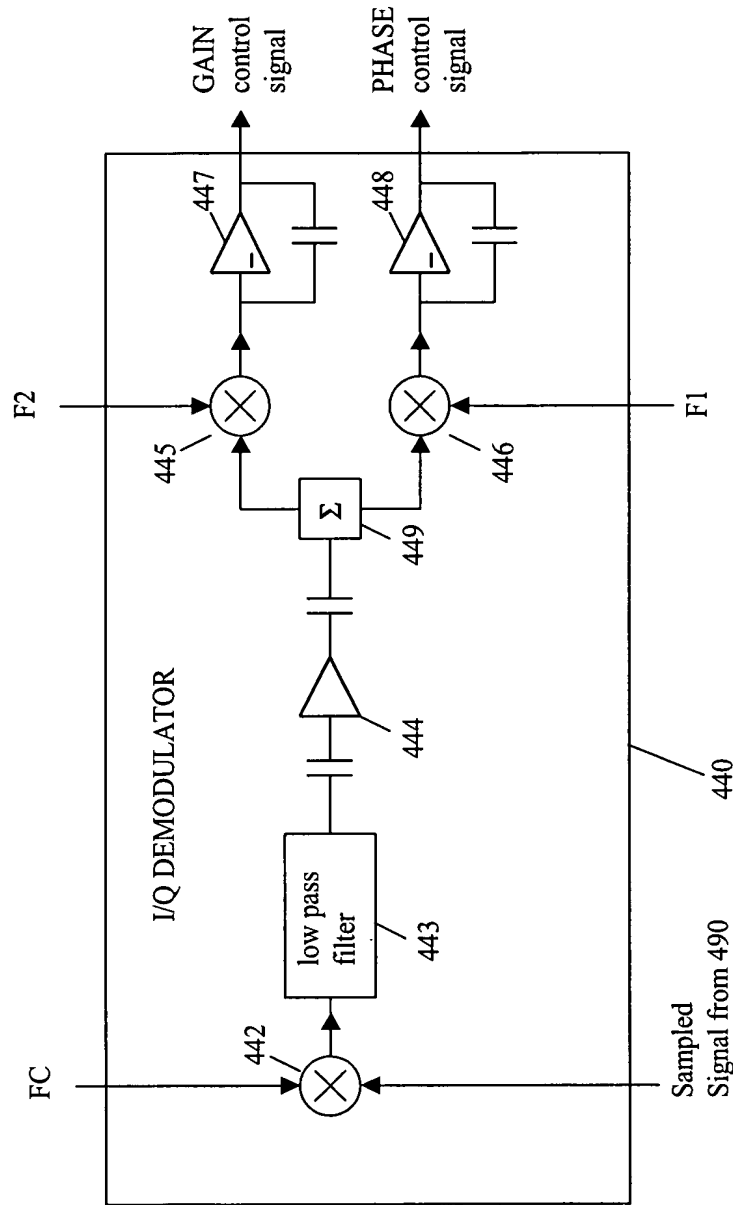
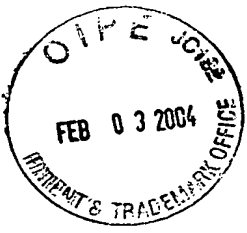


**FIG. 8**

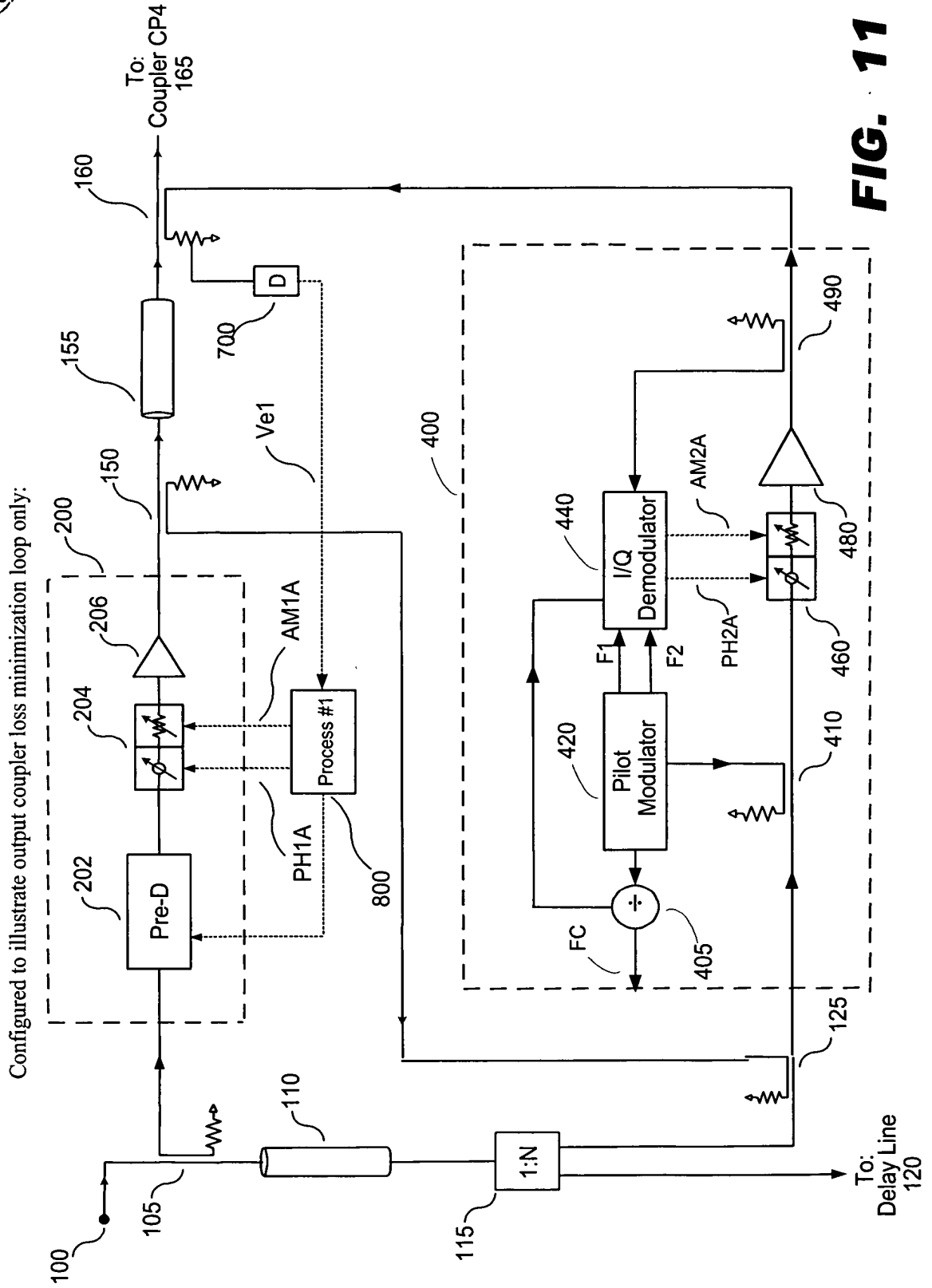
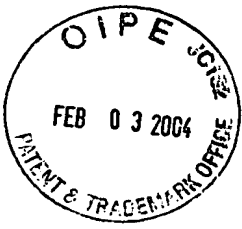




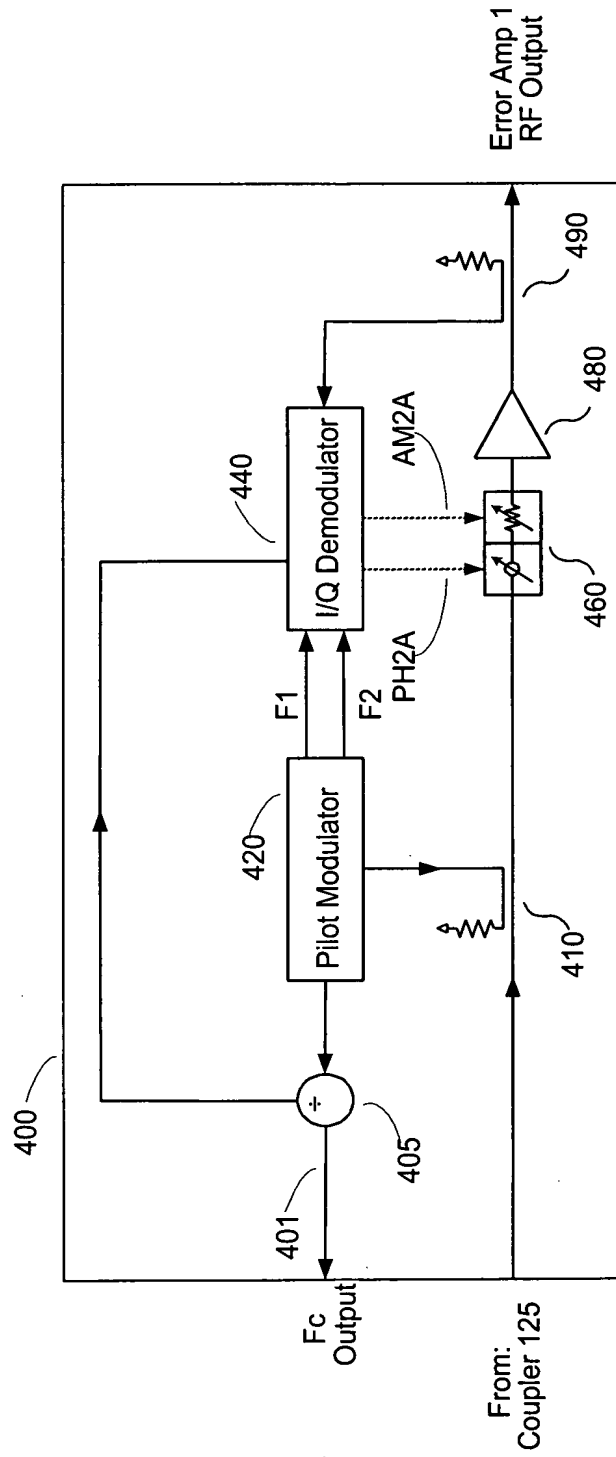
**FIG. 9**



**FIG. 10**

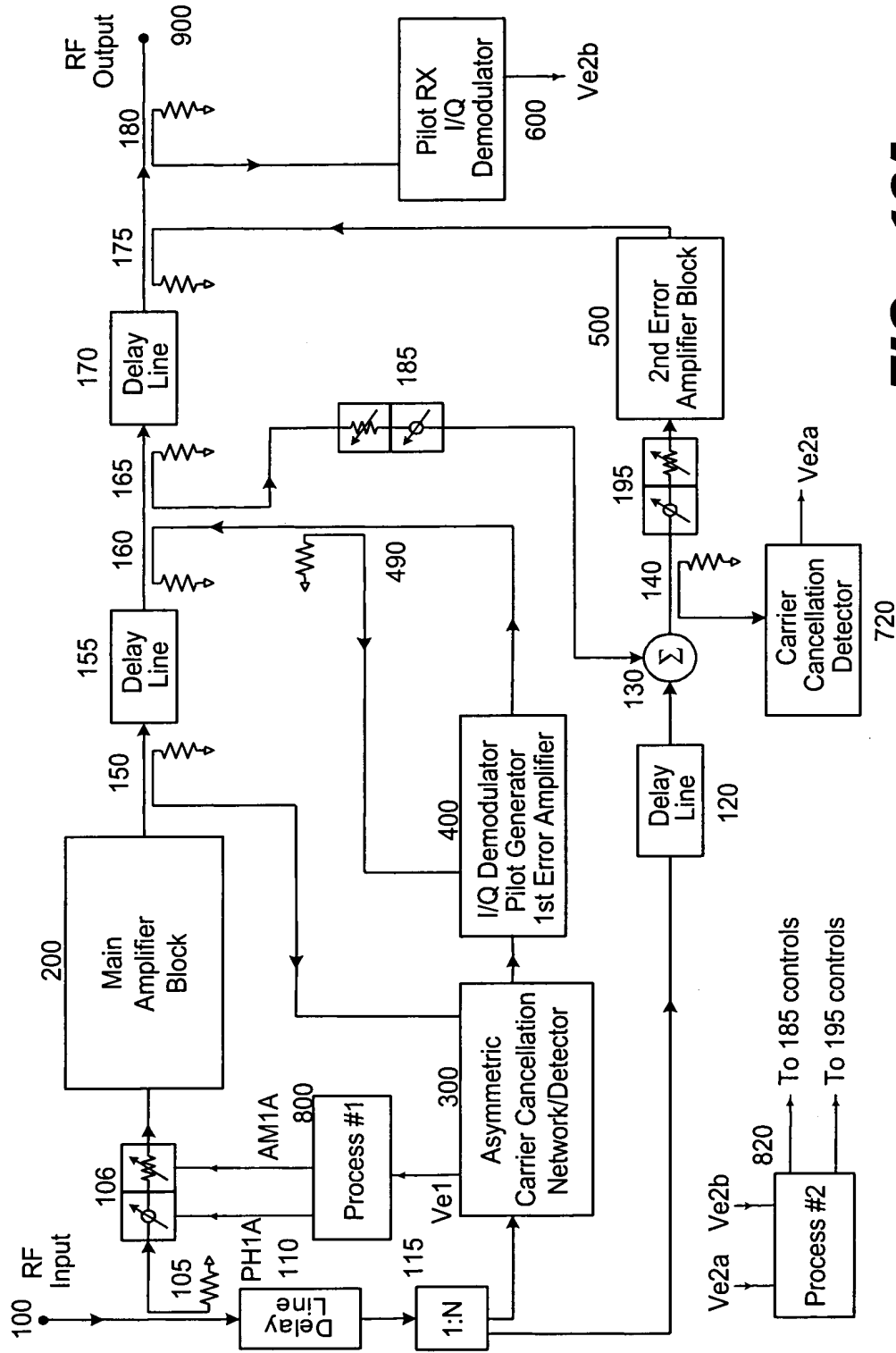


**FIG. 11**



**FIG. 12**





**FIG. 13A**









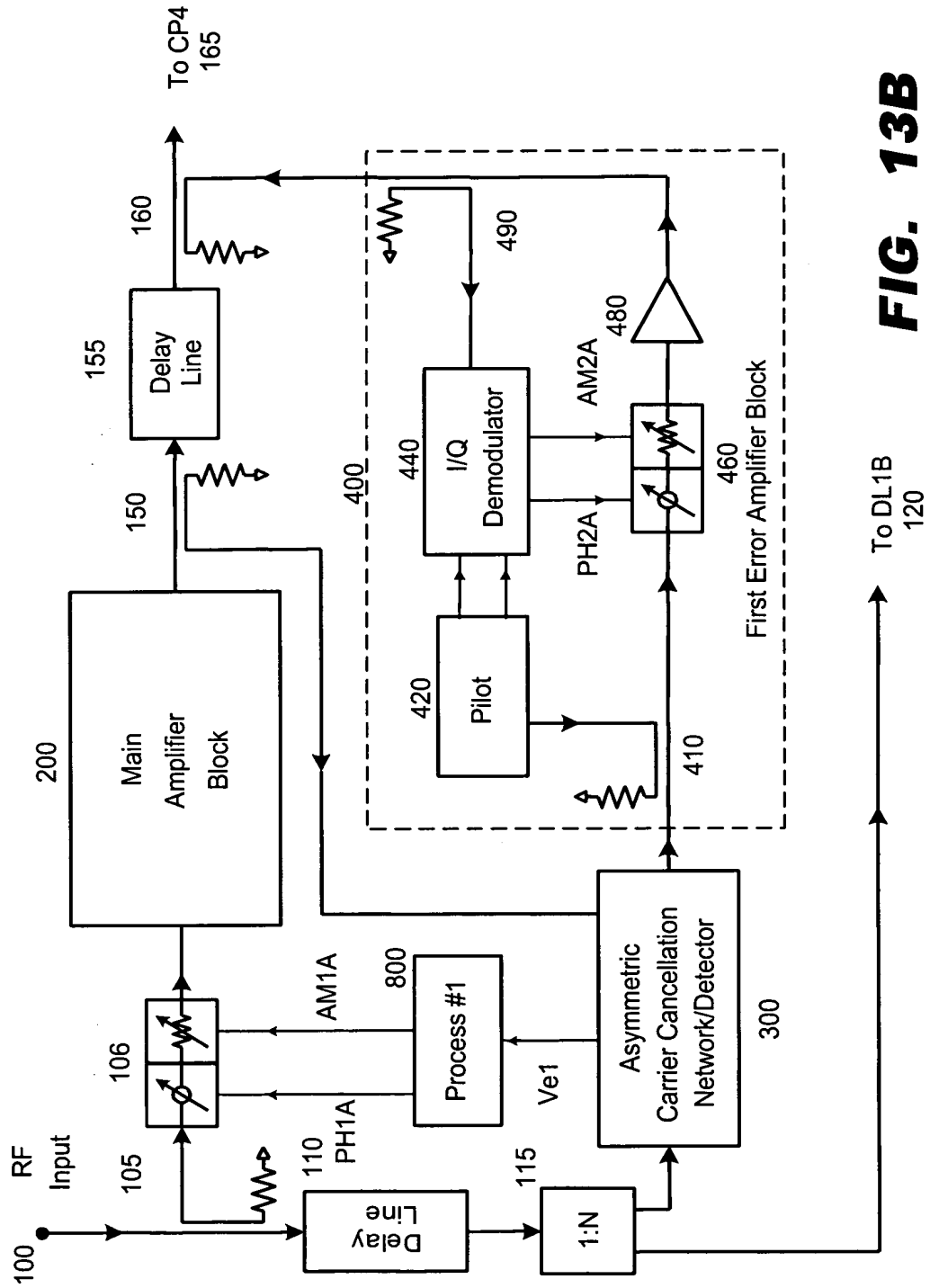
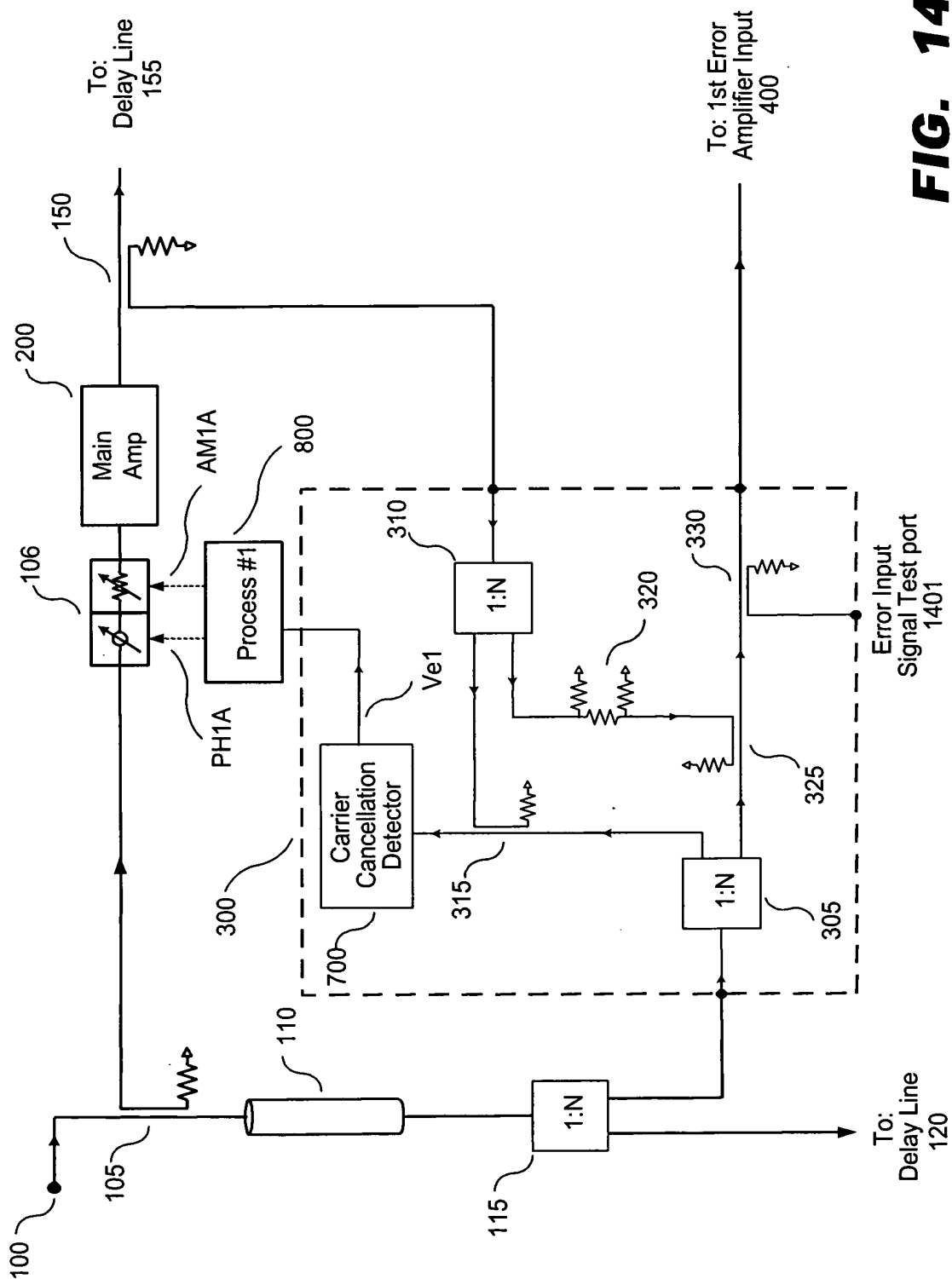


FIG. 13B



**FIG. 14**

The diagram illustrates a receiver architecture. The RF Input (100) enters a dashed box labeled 200. It passes through a Pre-D block (202), which outputs signal C to a Delay Line (105). The Delay Line (105) has two outputs: one goes to a 1:N block (115) and another goes to a Pilot block (420). The Pilot block (420) also receives signal S1 from the 1:N block (115). The output of the Pilot block (420) goes to an I/Q Demodulator (440). The I/Q Demodulator (440) has two inputs: one from the Pilot block (420) and another from a PH2A block (460). The output of the I/Q Demodulator (440) goes to an AM2A block (480). The output of the AM2A block (480) goes to a summing junction (Σ) at node 130. The summing junction (Σ) also receives input from a Delay Line (120). The output of the summing junction (Σ) goes to a Carrier Cancellation Detector (720). The Carrier Cancellation Detector (720) has two outputs: Ve2a and Ve2b. Ve2a is fed back to the PH2A block (460) via a 1:820 block. Ve2b is fed back to the Pilot block (420) via a 1:195 block. There are also other feedback paths involving delay lines (170, 185) and amplifier blocks (2nd Error Amplifier Block, 500).

**FIG. 15**